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L2: Entry 1 of 4 File: USPT Jun 17, 1997

DOCUMENT-IDENTIFIER: US 5640573 A
TITLE: Power management message bus for integrated processor

BSPR:
The present invention further contemplates a computer system comprising an integrated processor including a CPU core and a power management message unit coupled to the CPU core, wherein the power management message unit is capable of detecting an internal activity of the integrated processor and of providing an encoded value indicative of the internal activity on an external set of terminals. The computer system further comprises a power management message bus coupled to the external set of terminals, and a power management unit coupled to the power management message bus for managing power within the computer system.

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L7: Entry 1 of 1 File: USPT Feb 22, 2000

DOCUMENT-IDENTIFIER: US 6028488 A
TITLE: Digitally-controlled oscillator with switched-capacitor frequency selection

BSPR:
As related to clock generation, the increase in clock frequencies has in turn made the timing constraints for communication among the various integrated circuits more stringent. Particularly in systems that utilize synchronous operation and data communication among multiple integrated circuits, the timing skew between external system clocks and the internal clocks that control the operation of the integrated circuits must be reduced to very small margins.

BSPR:
Conventional systems generally utilize analog PLLs for on-chip generation and synchronization of internal clock signals from system reference clocks. Typical analog PLLs include a phase detector that compares the phase relationship of the reference clock to an internal clock, a charge pump and loop filter for setting an analog voltage corresponding to this phase relationship, and a voltage-controlled oscillator (VCO) for generating an output clock signal in response to the analog voltage from the charge pump and loop filter. In recent years, digital phase detectors have been used in on-chip PLLs in combination with the analog charge pump and filter, and the analog VCO; such PLLs have been referred to as "digital", but of course in reality these PLLs are hybrid digital and analog circuits.

DEPR:
Upon configuration of PLL clock generator 50 as noted above, operation begins with phase-frequency detector 64 comparing the relative position of a transition of the clock signal on line INCLK to a transition of the feedback clock signal on line FBCLK. The various components within PLL clock generator 50 will have been initialized by this time, for example by way of an enable signal and associated circuitry (not shown in FIGS. 4 through 9 for purposes of clarity), such that DCO 60 begins operation at an initial frequency, generating a feedback clock signal on line FBCLK. During the initial stages of the lock-in process, multiplexer 67 may be controlled to select the output of multiplexer 65 for use as the clock signal on line OUTCLK, if desired.

DEPR:
The PLL clock generator according to the present invention provides important advantages, not only in the generation of on-chip clock signals, but also in systems utilizing the same. Firstly, the output clock signal generated by the PLL clock generator is directly synthesized to have the desired frequency, rather than being derived from a high frequency source. This direct synthesizing enables the use of extremely small incremental frequency changes, selected by the implementation of capacitors with small sizes, without requiring the implementation of high frequency oscillators as used in conventional DCOs. Furthermore, the use of the binary-weighted switched capacitor array to synthesize the clock signal is extremely efficient in chip area, as compared to other direct synthesis oscillators, such as those using current controlled delay stages.

DEPR:
DSP 30 in this example is implemented by way of a modified Harvard architecture, and as such utilizes three separate data buses C, D, E that are in communication with multiple execution units including exponent unit 132, multiply/add unit 134, arithmetic logic unit (ALU) 136, and barrel shifter 138. Accumulators 140 permit operation of multiply/add unit 134 in parallel with ALU 136, allowing simultaneous execution of multiply-accumulate (MAC) and arithmetic operations. The instruction set executable by DSP 30, in this example, includes single-instruction repeat and block repeat operations, block memory move instructions, two and three operand reads, conditional store operations, and parallel load and store operations, as well as dedicated digital signal processing instructions. DSP 30 also includes compare, select, and store unit (CSSU) 142, coupled to data bus E, for accelerating Viterbi computation, as useful in many conventional communication algorithms.

DEPR:
DSP 30 in this example includes significant on-chip memory resources, to which access is controlled by memory/peripheral interface unit 145, via data buses C, D, E, and program bus P. These on-chip memory resources include random access memory (RAM) 144, read-only memory (ROM) 146 used for storage of program instructions, and data registers 148; program controller and address generator circuitry 149 is also in communication with memory/peripheral interface 145, to effect its functions. Interface unit 58 is also provided in connection with memory/peripheral interface to control external communications, as do serial and host ports 153. Additional control functions such as timer 151 and JTAG test port 152 are also included in DSP 30.

DEPR:
According to this preferred embodiment of the invention, the various logic functions executed by DSP 30 are effected in a synchronous manner, according to one or more internal system clocks generated by PLL clock generator 50, constructed as described hereinabove. In this exemplary implementation, PLL

clock generator 50 directly or indirectly receives an external clock signal on line REFCLK, such as is generated by other circuitry in the system or by a crystal oscillator or the like, and generates internal system clocks, for example the clock signal on line OUTCLK, communicated (directly or indirectly) to each of the functional components of DSP 30.

DEPR:
DSP 30 also includes power distribution circuitry 156 for receiving and distributing the power supply voltage and reference voltage levels throughout DSP 30 in the conventional manner. As indicated in FIG. 10, DSP 30 according to the preferred embodiment of the present invention may be powered by extremely low power supply voltage levels, such as on the order of 1 volt. This reduced power supply voltage is of course beneficial in maintaining relatively low power dissipation levels, and is in large part enabled by the construction and operation of PLL clock generator 50, which generates stable and accurate internal clock signals even with such low power supply voltages.

DEPR:
Referring now to FIG. 11, an example of an electronic computing system constructed according to the preferred embodiment of the present invention will now be described in detail. Specifically, FIG. 11 illustrates the construction of a wireless communications system, namely a digital cellular telephone handset 200 constructed according to the preferred embodiment of the invention. It is contemplated, of course, that many other types of communications systems and computer systems may also benefit from the present invention, particularly those relying on battery power. Examples of such other computer systems include personal digital assistants (PDAs), portable computers, and the like. As power dissipation is also of concern in desktop and line-powered computer systems and microcontroller applications, particularly from a reliability standpoint, it is also contemplated that the present invention may also provide benefits to such line-powered systems.

DEPR:
Microcontroller 226 controls the general operation of handset 200 in response to input/output devices 228, examples of which include a keypad or keyboard, a user display, and add-on cards such as a SIM card. Microcontroller 226 also manages other functions such as connection, radio resources, power source monitoring, and the like. In this regard, circuitry used in general operation of handset 200, such as voltage regulators, power sources, operational amplifiers, clock and timing circuitry, switches and the like are not illustrated in FIG. 11 for clarity; it is contemplated that those of ordinary skill in the art will readily understand the architecture of handset 200 from this description.

CLPV:
first and second reset transistors, each having a conduction path and a control terminal, the conduction paths of the first

reset transistor connected between a power supply voltage and the common node, and the conduction path of the second reset transistor connected between the common node and a reference voltage;

CLPV:
reset logic, having an input coupled to the output of the Schmitt trigger, and having outputs coupled to the control terminals of the first and second reset transistors, for turning on the first reset transistor responsive to a transition at the output of the Schmitt trigger indicating that the voltage at the common node has reached a first threshold of a logic level corresponding to the power supply voltage, and for turning on the second reset transistor responsive to a transition at the output of the Schmitt trigger indicating that the voltage at the common node has reached a second threshold of a logic level corresponding to the reference voltage.

CLPV:
first and second reset transistors, each having a conduction path and a control terminal, the conduction path of the first reset transistor connected between a power supply voltage and the common node, and the conduction path of the second reset transistor connected between the common node and a reference voltage;

CLPV:
reset logic, having an input coupled to the output of the Schmitt trigger, and having outputs coupled to the control terminals of the first and second reset transistors, for turning on the first reset transistor responsive to a transition at the output of the Schmitt trigger indicating that the voltage at the common node has reached a first threshold of a logic level corresponding to the power supply voltage, and for turning on the second reset transistor responsive to a transition at the output of the Schmitt trigger indicating that the voltage at the common node has reached a second threshold of a logic level corresponding to the reference voltage.

CLPY:
first and second reset transistors, each having a conduction path and a control terminal, the conduction path of the first reset transistor connected between a power supply voltage and the common node, and the conduction path of the second reset transistor connected between the common node and a reference voltage;

CLPY:
reset logic, having an input coupled to the output of the Schmitt trigger, and having outputs coupled to the control terminals of the first and second reset transistors, for turning on the first reset transistor responsive to a transition at the output of the Schmitt trigger indicating that the voltage at the common node has reached a first threshold of a logic level corresponding to the power supply voltage, and for turning on the second reset transistor responsive to a transition at the output of the Schmitt trigger indicating that

the voltage at the common node has reached a second threshold of a logic level corresponding to the reference voltage;

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L6: Entry 5 of 19 File: USPT Sep 12, 2000

DOCUMENT-IDENTIFIER: US 6119186 A
TITLE: Computer system with environmental manager for detecting and responding to changing environmental conditions

DEPR:
Informants 22 are receivers and generators of information regarding all aspects of operation of the computer system. Classes of informants shown in FIG. 3 include hardware and bus informants 22a, software informants 22b, user output informants 22c, user input informants 22d and script processing informants 22e, Particular informants 22 within the hardware class would include, for example, docking informants to detect and manage docking functions for a notebook computer, power informants to detect power sources and to automatically turn devices on and off, modem informants to detect and control different modem types (data, data/fax, data/fax/voice, cellular), printer informants to handle printer connections and print jobs, monitor the status of the parallel port for a printer which is directly connected to the computer, monitor network connected printers, monitor infra-red connections, and GPS informants which interface with a global positioning system (GPS). Bus informants would include, for example, informants for providing information and controlling network connections (direct connect and wireless), PC Card connections, SCSI connections and infra-red connections. Software informants would include environment informants to determine local environmental factors such as local area code, time zone, zip code and so on, scheduling informants to schedule activities at specific times, workspace informants to monitor activities in each workspace and maintain histograms to determine the most used user commands, and autostart informants to automatically launch applications based on usage and user choice.

DEPR:
FIG. 5a illustrates a diagram showing various detection mechanisms which could be used in conjunction with a notebook computer to provide environmental information, some or all of which could be used in a given situation. The notebook computer 70 has circuitry to receive signals from a GPS device 72, active/passive location device 74 or wireless network 76. Wired connections can be made to networks or external peripherals 78 through the computer's ports (serial/parallel) and buses (PC Card slots, option bays and other external bus connections). Other computers and devices, such as Personal Digital Assistants (PDAs, sometimes referred to as handheld or palmtop computers), can be coupled to the notebook computer 70, either

by wired or wireless connections. Internally, the notebook computer can reference information stored in various databases, such as a scheduling program, and the computer's time/date circuitry 82. The computer 70 can also detect its internal configuration of active programs and desktop configuration 84 (the configuration in which the user views and interacts with the programs).

DEPR:
PDAs, programmable calculators and personal organizers 80, such as those manufactured by Texas Instruments, Sony Corporation, US Robotics Corporation, Casio and Apple can exchange information with the notebook computer 70 through a port or through wireless transfer. Other accessories, such as the TIMEX DATALINK watch can receive information with the notebook computer. It would be possible to provide interfaces with other appliances, such as television sets, video tape recorders and alarm systems.

DEPR:
In decision block 136, the accumulated count for the program is used to determine the frequency at which the user loads the program while in the particular workspace. This frequency is set as a percentage and compared to a user defined threshold, Max %. If the number of counts in the current desktop exceeds Max % for that desktop, the user is prompted as to whether the application should be placed in an autolaunch list for the current desktop. If the user replies affirmatively, the application name is placed on an autolaunch list for the current desktop.

CLPV:
comparing said information to a threshold.

CLPV:
comparing said information to a threshold.

WEST

Generate Collection

L8: Entry 82 of 161 File: USPT Jun 9, 1998

DOCUMENT-IDENTIFIER: US 5763960 A
TITLE: Power supply controlled operation sequencing method and apparatus

BSPR:
A number of prior art devices are directed at controlling or resetting such electronic circuits via the generation of a logic or reset signal which may or may not be based upon the power supply voltage level. These devices are not intended to solve the problem of controlling the voltage provided to the electronic circuits, rather, they are directed toward controlling the function of the electronic circuits by providing specialized logic signals to specialized circuitry in the electronic circuits which in turn controls the operation of the electronic circuit. For example, U.S. Pat. No. 5,136,181 to Yukawa describes a power on reset circuit which generates a high level signal as a reset signal to an external circuit independent of the ramping of the power supply voltage upon actuating the power supply. Thus, power management problems created as the supply voltage is in transition are not addressed by Yukawa. Other devices require external reference voltages to enable control of their associated electronic circuits, for example, U.S. Pat. No. 5,587,684 issued to Salcedo, teaches a power down circuit for use with battery operated devices which may be distributed to and incorporated into the electronic circuits of the devices. In the Salcedo patent, an externally applied reference voltage is to used to control the power components of an analog circuit such as a ADC or DAC. The externally applied reference voltage is compared against a threshold voltage to control power provision to various stages of the electronic circuit. The requirement of the externally applied reference voltage to generate logic to control power switching to the circuitry requires supply voltage be available to the logic circuitry in order to enable power management functions, thus Salcedo also fails to address the problem of managing power during power supply transition.

WEST

Generate Collection

L8: Entry 62 of 161 File: USPT Apr 20, 1999

DOCUMENT-IDENTIFIER: US 5896261 A
TITLE: Power down protection circuit for an electronic device

DEPR:
During operation of the local device 102, the main control section 110 manages depletion of the power supply 114 according to power supply thresholds stored in the memory 113 and power management instructions stored in memory 117. In accordance with the power management instructions, the main control section 110 monitors the depletion of the power supply 114 via connection 116. The main control section 110 detects a voltage level of the power supply 114 and compares the voltage level to a low battery threshold or power down threshold. The power down threshold is stored in memory 113 of the power supply 114 and defines a voltage level below which the sections 106, 108, and 112 can only operate for a limited amount of time. When the voltage of the power supply 114 falls below the power down threshold and remains there for a predetermined time period (which is stored in memory 117), the main control section 110 initiates, according to the power management instructions, a controlled power down of the sections 106, 108, and 112 by communicating power down signals via connections 124, 118, and 130, respectively. In the illustrated embodiment, the power down threshold for a 3.6 V, 500 m.OMEGA., 500 mA.multidot.hour supply is approximately 2.85 V, the predetermined time period is approximately 35 ms, and the time it takes to execute the controlled power down is approximately 800 ms.

DEPR:
The comparator 164 includes ports 172-176. Port 172 is a supply input and is coupled to connection 116 to receive power from the power supply 114. Port 173 is a ground input and is coupled to the electrical ground 171. Port 174 is voltage input and is coupled to connection 116 via a resistive element 178 so as to receive a voltage level of the power supply 114. Resistive element 178 provides a voltage drop necessary to match the power supply 114 to port 174 and is preferably a resistor having a value of approximately 10 k.OMEGA., or other suitable alternative. Port 175 is voltage input and is coupled to port 170 of the voltage reference 162 via a resistive element 180. Resistive element 180 provides a voltage drop necessary to match the reference voltage level supplied by the voltage reference 162 to port 175 and is preferably a resistor having a value of approximately 11 k.OMEGA., or other suitable alternative. Port 176 is a signal output and is coupled to port 175 via a resistive element 181. Resistive element 181 sets a

level of hysteresis to prevent rapid transitioning between signal output levels at port 176 and is preferably a resistor having a value of approximately 100 k.OMEGA., or other suitable alternative. In the illustrated embodiment, the comparator 164 is an analog comparator or suitable alternative. In operation, the comparator 164 compares the voltage levels received at ports 174 and 175. When the voltage level at port 174 equals or exceeds the reference voltage level at port 175, the comparator 164 generates a low voltage output signal at port 176. When the voltage level at port 174 falls below the reference voltage level at port 175, the comparator 164 generates a high voltage output signal at port 176.

CLPR:
11. An electronic device according to claim 9 wherein the power down protection circuit comprises a comparator to compare a voltage level of the power supply and a reference voltage level indicative of the threshold.

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Generate Collection

L8: Entry 54 of 161 File: USPT Jul 27, 1999

DOCUMENT-IDENTIFIER: US 5930517 A
TITLE: Data processing system with separable system units

DEPR:
The docking station also has means for monitoring the state of charge of the rechargeable battery 10. This consists primarily of a sensor 11 and a power manager 15. The sensor 11 measures the voltage of the rechargeable battery 10. In addition, the sensor 11 compares the measured voltage of the rechargeable battery 10 with predetermined threshold values. The first threshold value corresponds to 10% of the energy of the rechargeable battery in the fully charged state. The second threshold value corresponds to 5% of the energy of the rechargeable battery in the fully charged state.

DEPR:
If the sensor 11 determines that the value has fallen below the first threshold value a signal is sent to the power manager 15 through the lead 12. This causes the power manager 15 printer 18 belonging to the docking station 1 to be switched off. This serves to save the energy of the rechargeable battery 10.

DEPR:
With a further drop in the voltage of the rechargeable battery 10 to below the second threshold value, a signal is sent through the lead 13 of the sensor 11 to the power manager 15. The result of this is that the power manager 15 generates the release signal, which is transmitted over the lead 16 and the computer connection 4 to the notebook PC 3. The release signal corresponds to the release signal which is produced by actuating the release button of the known docking station.

DEPR:
When the rechargeable battery voltage falls to 0, there is, of course, some residual energy remaining in the battery 17. This residual energy cannot, however, be withdrawn, without damaging the battery 17. In this case, a signal is consequently transmitted through the lead 14 from the sensor 11 to the power manager 15, the effect of which is to switch off the docking station. Before the docking station is switched off the user receives no further communication.

DEPR:
If the docking station is connected to the mains by way of the cable 8 after the rechargeable battery voltage falls below the first threshold value, the battery voltage 10 will increase again. After the 5% threshold value is exceeded, the sensor

again. After the 5% threshold value is exceeded, the sensor will no longer transmit any further signal through the lead 13, so that the periodic issuance of the disconnection signal by the power manager 15 through the lead 16 will cease.

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Generate Collection

L8: Entry 36 of 161 File: USPT Feb 15, 2000

DOCUMENT-IDENTIFIER: US 6025695 A
TITLE: Battery operating system

DEPR:
The Wake-Up Comparator is simply a voltage comparator which is turned on once every 500 msec cycle to roughly measure the full pack voltage. This is not an A/D measurement, just a rough measurement of the pack voltage using a simple resistive divider circuit. The pack voltage is then compared to the internal band-gap reference (1.25V nominal).

DEPR:
Sleep Mode is exited only via the Wake-Up Comparator Circuit which monitors the pack voltage. The smart battery device of the present invention is intended for use with an intelligent host device such as a portable computer, portable video camera or cellular telephone having a system management bus and a smart charger, or an intelligent host device having a system power manager that can receive and send data over a system management bus.

DEPR:
As shown in FIG. 3, whenever the analog signals representing battery voltage, current, and temperature are obtained, they are input into an ASIC multiplexor or switching network 55 which enables only one analog signal at a time to be input to the A/D converter 60 for digital conversion. The switching network acts in conjunction with digital logic circuitry for informing the A/D converter, via line 55', shown in FIG. 3, of the amount of integration cycles to perform depending upon the type of measurement to be converted. For instance, more integration cycles are needed when making a current measurement conversion to ensure a higher bit resolution as compared to when a voltage or temperature measurement is being converted, as will be explained in further detail below with respect to FIG. 8.

DEPR:
To monitor for the first of these end-of-charge conditions, the processing module, using the battery voltage sensing means and the analog-to-digital convertor, determines a digital value representing battery voltage, and the processing module then compares that newly determined digital value to a battery voltage data value currently stored in the processor memory. On the one hand, if this new data value is larger than that stored data value, then that currently stored data value is replaced

in the processor memory with the new data value. On the other hand, if the new data value is less than the currently stored battery voltage data value, then the difference between these two data values is compared to v. If that difference is greater than v, then the processing unit generates a signal and transmits that signal to a data terminal indicating that an end-of-charge condition has been detected.

DEPR:
Normally, transistors 89a and 89b are off in the sleep mode, and once every 500 milliseconds these transistors are turned on by a trigger signal 77a. In particular, transistor 89b is turned on by a signal 77b, which is output from inverter 72, to develop a path to ground to enable the voltage of the network to appear at the first comparator input. In addition, the enable line 15a receives signal 77a to simultaneously enable the comparator to compare the voltages applied to the comparator inputs.

DEPR:
FIG. 21, learn.sub.-- cells, is a routine to determine the number of cells connected in the battery pack. Generally, this routine initializes the number of cells for the battery at zero, and then compares the measured voltage at each multiplexer state (starting with 00) with a reference voltage, if the measured voltage is less than the reference voltage, it increments the assumed number of cells and the multiplexer state until the measured voltage is less than the reference voltage. The first step 2110 initializes the variable cells, which reflects the number of cells in the pack, to 0. The next step 2112 initializes the variable UMUX, which reflects the state of the input to the multiplexer, to zero (see the column in the upper right corner of FIG. 21). The next step 2114 sets the bit STC to 1, which starts the ADC converter. The next decisional block 2116 determines when the flag or bit CC, which reflects the completion of the A/D conversion, and when the ADC converter is finished that flag is set equal to 1.

DEPR:
FIG. 21a, learn.sub.-- cells, is a routine to determine the number of cells connected in a NiMH battery pack. Generally, in this cell learning routine when the maximum voltage conceivable for any string of cells is exceeded, it assumes that the string must be at least one cell more. The routine counts up incrementally in this fashion until the voltage is reasonable for the presently assumed number of cells in the string. It requires charging a battery pack to near full capacity to learn the correct number of cells. The initialization routine initializes the number of cells for the battery at 4, and then the learn.sub.-- cells routine compares the measured voltage with a reference voltage (U.sub.-- SWITCH.sub.-- 1 (a constant of 1650 mV) times the member of cells). If the measured voltage is greater than the reference voltage, it increments the assumed number of cells until the measured voltage is less than the reference voltage. The first step 2140 determines if the number of cells is less than MAXCELLS (a constant 10), and if so at step 2142 determines if the measured voltage U is greater

than U.sub.-- SWITCH.sub.-- 1 times cells, and if so at step 2144 increments the number of cells. The routine then returns to step 2140 and proceeds therethrough again until either of the conditions of steps 2140 or 2142 is false, and then exits the routine at 2142.

DEPR:
At step 4810, the processor makes two comparisons. First, the processor the compares the battery voltage to the product of a value U.sub.-- STANDBY.sub.-- 1 and the cells value; and second, the processor determines whether sample is equal to 1. If the battery voltage is less than or equal to the above-mentioned product, and sample is equal to 1, then the processor enters the sleep mode. To do this, at step 4812, ENA, LEDIO and LOMOD are all set to zero, and PRLOEN is set equal to 1. The processor then exits this routine. The processor also exits this routine if, at step 4810, sample is not equal to 1 or the battery voltage is greater than the product of cells and U.sub.-- STANDBY.sub.-- 1.

DEPR:
After step 4928, the processor, at step 4930 determines of the DT.sub.-- UTIMER has timed out. If this timer has timed out, the processor, at step 4932, then compares the present battery voltage to the maximum stored battery voltage, UMAX. If U is greater than UMAX, the battery voltage is increasing and UMAX is updated; while if U is not greater than UMAX, the battery voltage is not increasing and .DELTA.V is calculated. Specifically, UMAX is updated at step 4934 by being set equal to U; and .DELTA.V is calculated at step 4936 by being set equal to UMAX -U. After either step 4934 or step 4940, the DU TIMER is reset at step 4940, and the processor then moves on to step 4942.